REMARKS/ARGUMENTS

Regarding amendments to the claims:

Claims 1 and 4 are amended to overcome the objections set forth on the following detailed Office action and to emphasize the characteristics of the claimed invention. No new matter is entered by the above amendments.

Regarding rejections under 35 U.S.C. 102, 35 U.S.C. 103, and 35 U.S.C 112: Examiner:

1. **Claims 1-6 are rejected under 35 U.S.C 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 1 is vague and indefinite in describing the position of the dielectric layer and polysilicon layer relative to the substrate when stating "removing portions of the polysilicon layer and the dielectric layer down to the surface of the substrate". Claims 1 and 4 recite the limitation "the portions of the polysilicon layer" and there is insufficient antecedent basis for "the portions" in the claims.

Response:

Claims 1 and 4 are amended to overcome this rejection. According to the amended claim 1, a method of forming a polysilicon resistor, the method comprising: providing a substrate, the substrate comprising a dielectric layer; forming a polysilicon layer on the dielectric layer; doping the polysilicon layer with first type dopants and second type dopants; defining a polysilicon resistor pattern on the polysilicon layer and removing the polysilicon layer and the dielectric layer outside the polysilicon resistor pattern down to

the surface of the substrate, the remainder of the polysilicon layer comprising at least a high resistance region and a low resistance region; and forming a salicide layer on the remainder of the polysilicon layer within the low resistance region.

2. **Claims 7-9 are rejected under 35 U.S.C 102(b) as being anticipated by Bourassa (US Pat. 4658378).**

Bourassa discloses the method of forming a high resistance region of a polysilicon resistor comprising providing a substrate, the substrate comprising a dielectric layer, forming a polysilicon layer on the dielectric layer, and doping the polysilicon layer to form a low resistance region and a high resistance region, where N-type and P-type dopants having the same order of magnitude are used to form the high resistance region.

Response:

According to claim 7, the claimed invention teaches a method of forming a high resistance region of a polysilicon resistor, in which the method comprising: providing a substrate, the substrate comprising a dielectric layer; forming a polysilicon layer on the dielectric layer; and doping the polysilicon layer with first type dopants and second type dopants, thus forming the high resistance region on portions of the polysilicon layer. In contrast to the claimed invention, Bourassa first utilizes a first type dopant to dope the central region (34) of a polysilicon layer, then utilizes a second type dopant to dope the two side regions (36 and 38) corresponding to the central region, and utilizes the different dopant concentration of each region to adjust the resistance of the polysilicon resistor. Additionally, the central area (34) may also include both types of dopants, as suggested in column 4, line 56 to column 5, line 5. Under the condition when the central area of the polysilicon layer include both types of dopants whereas the two side regions include only one type of dopant, a PN junction will be formed between the central region (34) and the two side regions (36 and 38). In contrast to Bourassa, the polysilicon resistor of the

claimed invention is formed by doping the polysilicon layer with a first type dopant and a second type dopant simultaneously, in which the high resistance region and the low resistance both includes two types of dopants with equal concentration. Consequently, no PN junction is formed in the claimed invention.

According to Chapter 2112 in the MPEP, in relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flows from the teachings of the prior art. Since the inherency of a method of forming a high resistance region of a polysilicon resistor does not flow from the teachings of Bourassa, claim 7 should be novel based on the above analysis, and since claims 8 and 9 are depended upon claim 7, claims 8 and 9 should be allowed if claim 7 is allowed. Reconsideration of claims 7-9 is politely requested.

3. Claims 1-6 and 10-13 are rejected under 35 U.S.C 103(a) as being anticipated by Bourassa (US Pat. 4658378) in view of Kim (US Pat. 5780333).

a. Regarding claims 1-3, Bourassa teaches the element as set forth immediately above, but the reference does not teach the method of removing portions of the polysilicon layer and dielectric layer to the surface of the substrate. Kim shows the method of removing polysilicon and dielectric layers to the surface of the substrate.

Response:

According to claim 1, the primary characteristics of the claimed invention is to utilize two different types of dopants simultaneously to adjust the polysilican resistance in the high resistance region of a polysilicon resistor, and to use the formation of salicide layer to reduce the polysilicon resistance in the low resistance region of the polysilicon resistor. Despite the fact that Kim teaches a method of removing polysilicon and dielectric layers to the surface of the substrate, the combination of Kim and Bourassa never suggested the characteristics of the claimed invention. Hence, claim 1 should be allowed and since claims 2 and 3 are depended

upon claim 1, claim 2 and 3 should be allowed if claim 1 is allowed. Reconsideration of claims 1-3 is politely requested.

b. Regarding claims 1, 4, 6, 10, 11, and 13, Bourassa teaches the elements as set forth above, but the reference does not teach the method of forming a salicide block on portions of the polysilicon with high resistance and forming a salicide layer on portions of the polysilicon layer with low resistance on either side of the high resistance region. Kim shows the use of the salicide block over the high resistance region of the resistor to insulate it and a salicide layer at either end of the resistor to be used as electrical contacts.

Response:

As described previously, the the primary characteristics of the claimed invention is to utilize two different types of dopants simultaneously to adjust the polysilican resistance in the high resistance region of a polysilicon resistor, and to use the formation of salicide layer to reduce the polysilicon resistance in the low resistance region of the polysilicon resistor. Despite the fact that Kim teaches the use of the salicide block over the high resistance region of the resistor and a salicide layer at either end of the resistor, Kim never teaches the means of utilizing the formation of a salicide layer via the low resistance region to reduce the polysilicon resistance in the low resistance region. Hence, claim 1 should be allowed and since claims 4, 6, 10, 11, and 13 are depended upon claims 1 and 7, claims 4, 6, 10, 11, and 13 should be allowed if claims 1 and 7 are allowed.

c. Regarding claims 5 and 12, Bourassa teaches the elements as set forth above, but the reference does not teach the method of forming an inter layer dielectric on the substrate comprising a contact hole to the salicide layer and a conductive layer on portions of the inter layer dielectric and within the contact hole. Kim shows the use of an inter layer dielectric on the substrate, which is etched to form contact holes connecting to the salicide layer, and a metal layer deposited on portions of the dielectric and within the contact holes.

Response:

Since claims 5 and 12 are depended upon claims 1 and 7, claims 5 and 12 should be allowed if claims 1 and 7 are allowed.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)